## REMARKS

### *Summary Of The Office Action & Formalities*

Claims 1-5 are all the claims pending in the application. By this Amendment, Applicants are amending claim 1. No new matter is added.

Applicants thank the Examiner for acknowledging their claim to foreign priority and for confirming that the certified copy of the priority document was received.

Applicant is amending the Specification as suggested by the Examiner to overcome the Examiner's objection and to remove the requirement to label Figure 4B as prior art.

The prior art rejections are summarized as follows:

1. Claims 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wong, et al.

2. Claims 2, 3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong in view of (USP 5,467,347) to Petersen.

Applicants respectfully traverse.

### *Claim Rejections - 35 U.S.C. § 102*

*1. Claims 1 and 4 In View Of Wong, et al.*

In rejecting claims 1 and 4 in view of Wong, et al., the grounds of rejection are essentially the same as those set forth in the previous Office Action of September 18, 2002. In response to Applicant's arguments traversing these grounds of rejection as set forth in the Amendment of December 18, 2002, the Examiner states:

> Regarding claim 1, Applicant argues that the reference used to show Wong teaches setting the value of m equal to n for the m x

n matrix is directed to the three-stage architecture of Fig. 2, and thus, is not directed to the two-stage architecture of Fig. 1. The reference to Fig. 2, however, was made to indicate a configuration known in the architecture of Fig. 1. The reference to Fig. 2, however, was made to indicate a configuration known in the art which specifically utilizes values of m equal to n. Further explanation of Wong teaching setting the value of m equal to n, however, is provided in the following. Applicant further argues that Wong teaches away from having m=n by stating that it is preferred to have the ratio e=m/n to be greater than 1. Wong, however, does *not* teach away from having m=n. Rather, with respect to Figure 1, Wong discloses three different techniques are used in the art to reduce the loading within the switching fabric, only one of which comprises having values of m greater than n. A first technique involves providing buffers at the output of first-stage switch (page 708, col. 2, lines 4-5). A second technique is called "grouping" (lines 3-8) wherein more than one line, e.g. *r* lines, is provided for each path between the two stages. Wong discloses that the grouping technique is often preferred for reducing the possibility of congestion (lines 7-8). Wong further discloses a third technique called "input-expansion" (lines 9-16) wherein the ratio e=m/n is designed to be greater than 1. Wong notes that r and e are in fact related wherein if the value of r is adjusted, the value of e should also be adjusted in order to maintain comparable performance. While Wong uses an example of having a group size r=8 and choosing a corresponding input-expansion e=2 to provide close to 100% throughput for the given group size, r and e values are not limited to this first example. The teachings of Wong in fact are directed towards reducing the input-expansion ratio, e, while achieving comparable packet loss performance (page 710, col. 1, lines 1-5), which reduces the amount of hardware interconnections. In the invention of Wong (Figure 4), the two-stage architecture of Figure 1 configured with first-stage and second-stage switching grouped into partitions (e.g., Figure 3; see also page 709, col. 2, lines 4-6), yielding a three-stage Dilated-Banyan switch, is utilized with the addition of an overflow switch (v x v, see Figure 4). Wong specifies m is set to be greater than *or equal* to n (page 710, col. 1, lines 8-10) and further discloses a simulation wherein e=1 (i.e., m=n) in Table 1(a) (page 711). Thus, Wong clearly teaches an embodiment as described in claim 1 wherein the value of m is equal o the value of n.

Office Action at pages 4-5. Applicant respectfully disagrees.

The grounds of rejection are not based on a fair reading of Wong et al., but rather on improper hindsight using Applicant's own disclosure as a road map to construct Applicant's invention in light of the very general disclosures in the prior art.

In alleging that Wong et al. discloses the switching architecture recited in claim 1, the grounds of rejection selectively lift certain features and guess as to others without having any clear teaching or suggestion for doing so (see, for example, the alleged relationship between K and l ("along the same logic k=l, thus n=m=s=p=R and k=l=N," and the relationship that m = n = 1). Applicant maintains that a fair reading of Wong et al. would not lead one skilled in the art to the architecture asserted by the Examiner, but, to the contrary, would lead one away from such an arrangement for the reasons set forth in Applicant's last response that remain pertinent to the present rejection and which are fully incorporated herein by reference.

Applicant argued in the December 18, 2002 Amendment that Wong et al. does not teach that "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input; and in that each output . . . of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs . . . of the outlet stage exclusively associated with that output." In response, the Examiner states:

> Wong teaches *grouping* (see Figure 1) wherein more than one line, e.g. *r* lines, selected from a particular grouping of r lines, are provided for each path between the inlet and outlet stages. That is, Wong teaches each input of the inlet stage (n) can be connected to an output of the inlet stage (at m, one of the lines of a

> corresponding grouping of r lines) selected from only Q outputs (r outputs) exclusively associated with that input (n); and that each output of the outlet stage (p) can be connected to an input of the outlet stage (at s, one of the lines of a corresponding grouping of r lines) which can be selected only from Q' inputs (r inputs) of the outlet stage exclusively associated with that output (p).
>
> Regarding claim 4, Applicant argues that the rejection is based upon an assumption that n'=1, and Wong lacks sufficient specificity to constitute such an anticipation. While the teachings of Wong do not require specifically n=1 or n'=1, Figure 3 accommodates such an embodiment as evidence by "..." between the first (1) and kth (k) inputs, outputs, etc. That is, Figure 3 is not limited to a specific number of inputs, outputs, etc. Moreover, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider,148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Furthermore, in reference to the language of claim 4, "each of the inlet stage has single input and R outputs", using the above-mentioned grouping method, Wong provides each single input (n) having R outputs (r or r').

Office Action at page 5. Applicant respectfully disagrees.

In particular, the grounds of rejection do not point to any disclosure in Wong et al. that teaches or suggest the exclusive relationship recited in claim 1 between each input of the inlet stage and the associated Q outputs. As Applicant already noted, at page 1, lines 28-30 of Applicant's specification, in a Clos network, each of the intermediate stage matrices is connected to one of the outputs of each of the inlet stage matrices. That is, in a three-stage Clos network, every first or inlet stage switching module has one and only one connection to each of the second

stage modules. This is also true for the third stage switching module. Moreover, each of the input links for each inlet matrix can be associated with any of the output links of that matrix. Similarly, each of the output links for each last stage matrix can be associated with any of the input links of that matrix. Furthermore, referring to Fig. 2 of the present application, for example, outputs $213_{1,1}$ through $213_{1,N}$ of the first inlet stage matrix $211_1$ are exclusively associated with inputs $212_1$. Similarly, outputs $213_{R,1}$ through $213_{R,N}$ of the first inlet stage matrix $211_1$ are exclusively associated with inputs $212_R$.

Contrary to the Examiner's assertion, however, Wong et al. makes no reference (i.e., not teaching or suggestion) as to whether there is any exclusive relationship, in the manner recited in claim 1, between the input and outputs of the first stage matrices. The matrices are graphically shown without any path links within them, and the text of the reference makes no mention of an exclusive relationship. For example, the first through last inputs of the first stage matrix (1) may be associated with the first grouping of outputs r of that matrix. There simply is no indication in the reference as to what is the precise relationship, exclusive or otherwise. Accordingly, Applicant maintains that the Examiner cannot rely on Wong et al. for such a specific teaching or suggestion.

Finally, Applicant is amending claim 1 to recite that the device for switching is "further configured so that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage." Support for this feature can be found at page 7, paragraph beginning at line 21. Wong et al. clearly does not teach or suggest this feature. To the contrary, referring to Fig. 1 of the reference, if one assumes, for the sake of argument, that for a given first stage (n x m)

matrix each input is exclusively associated with a particular group r of outputs (which the Examiner appears to be asserting in the rejection as noted above), then clearly each of these inputs is not associated with each second stage (s x p) matrix. The opposite is in fact illustrated in Fig. 1 of Wong et al.

Regarding claim 4, Applicant maintains that Wong simply lacks sufficient specificity to constitute anticipation of claim 4. The Examiner admits as much in the present Office Action, stating that "Figure 3 is not limited to a specific number of inputs, outputs, etc." Office Action at page 6. That is, the Examiner acknowledges that Wong et al. fails to provide the particular architecture recited in the claims, but appears to allege that through experimentation one skilled in the art would achieve the claimed configuration. Clearly, an invitation to experiment cannot amount to the requisite disclosure to suggest a particular architecture, let alone anticipate such an architecture.

The Examiner adds, "it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Applicant." Office Action at page 6. However, "[a] particular parameter must first be recognized as a result-effective variable . . . before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." MPEP § 2144.05(b). The grounds of rejection do not address this threshold inquiry at all, and any burden shifting at this time is clearly premature.

In view of at least the foregoing distinctions, claims 1 and 4 are believed to be allowable over the prior art, and the Examiner is kindly requested to reconsider and withdraw the rejection of these claims.

***Claim Rejections - 35 U.S.C. § 103***

*1. Claims 2, 3 and 5 In View Of Wong et al. to Petersen.*

In rejecting claims 2, 3 and 5 in view of Wong to Petersen, the grounds of rejection state

> Wong teaches various architecture for ATM switching, and particularly for fast-packet switching in order to provide widespread use of broadband communications. Wong identifies the primary goals for ATM switching which include: minimizing the number and size of the switches needed maintaining, high throughput and low loss possibility, and maintaining packet sequence (page 708, col. 1, "Introduction"). Wong attempts to achieve as much of these goals as possible using three-stage banyan architecture with overflow switching. Petersen also recognizes the need for improved ATM switching (col. 1, line 9 - col. 2, line 39) and states that while other prior art is oriented towards developing switchcores of greater magnitude (including banyan related architecture coupled with buffering, as taught by Wong) in order to meet demands of, for example, broadband communication, a need exists for access control to improve size, capacity/throughput, and loss problems (col. 2, lines 24-39) commonly experienced with this existing art. In particular, the invention of Petersen eliminates the need for large buffers in the switchcore (col. 3, lines 13-17), reducing size requirements. Additionally, Petersen teaches a switchcore matrix having a plurality of rows, columns and crosspoints for providing both multicast and broadcast capabilities (col. 2, lines 42-62), significantly improving capacity/throughput. Further, Petersen teaches a switchcore matrix with access control and wherein a plurality of switchcore matrixes are link-coupled to enhance switch performance (col. 2, lines 58-62), wherein cell loss probability can be reduced and control can be provided for maintaining packet sequence. Finally, the invention of Petersen provides simplicity such that it may be constructed on a single integrated circuit,

> making it ideal for manufacture and application. Thus, the access control an d crosspoint features of the invention of Petersen clearly provide improvements over Wong, wherein the goals specified by Wong are achieved by Petersen resulting in significant improvements in ATM switching. Accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Petersen to the device of Wong in order to provide improved ATM switching as discussed above.

Office Action at pages 6-8. Applicant respectfully disagrees.

At best, the combination of Wong et al. and Petersen is an invitation to perform further research in switching architecture, but clearly lacks the specificity, including the disclosure of result-effective variables for constructing the switching devices of claims 2, 3, and 5.

Moreover, claims 2, 3 and 5 are believed to be allowable at least by reason of their respective dependencies.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

**The specification is changed as follows:**

**The paragraph added by Applicant's previous amendment at page 6, beginning at line 34 is amended as follows:**

Figures 4A and 4B show an advantageous structure based on the network from Figure 3, with Fig. 4A showing a known device allowing narrowband transfers, and Figure 4B showing a device according to the invention [and which allows wide band transfers], this latter device being able to be derived from incomplete prior art matrices and by restricting routing in these derived prior art matrices to allow broadband transfers (Figure 4B) [and narrowband transfers (Figure 4A)]; and

IN THE CLAIMS:

**The claims are amended as follows:**

Claim 1. (Twice Amended) A device for switching ATM cells establishing a single path per virtual circuit, having N.R inputs and N.R outputs, N and R being two integers not less than two, the device comprising at least two stages, including an inlet stage comprising a plurality of matrices (21; 31; $411_1$, ..., $411_R$) and having R.N sets of Q outputs ($213_{11}$; $313_{11}$; $413_{11}$) and an outlet stage comprising a plurality of matrices (22; 33; $421_1$, ..., $422_1$, ...) and having R.N sets of Q' inputs ($222_1$; $332_{1,1}$; $423_{1,1}$),

characterized in that for the flow of data carried by any intermediate link ($213_i$, $222_j$; $313_i$, $332_j$, $413_i$, $423_j$) that is part of the single path set up between an input and an output to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input ($212_1$; $312_1$; $412_1$) of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs ($213_{11}$, ..., $213_{R1}$; $313_1$, ..., $313_{1R}$; $413_{11}$, ..., $413_{1R}$) exclusively associated with that input; and

in that each output ($223_1$; $333_1$; $442_1$)of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs ($222_{11}$, ..., $222_{1R}$; $332_{11}$, ..., $332_R1_1$; $423_{11}$, ..., $423_{1R}$) of the outlet stage exclusively associated with that output; and

further configured so that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage.